AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) A data processing apparatus comprising:

arbitration logic; and

a data processor core, said data processor core comprising:

a memory access interface portion for performing data transfer operations between an external data source and at least one memory associated with said data processor core;

a data processing portion for performing data processing operations;

a read/write port for transferring data from said processor core to first and second buses, said first and second buses providing data communication between said processor core and said at least one memory, said at least one memory comprising first and second memory portions, said first bus providing exclusive access to said first memory portion and said second bus providing exclusive access to said second memory portion, wherein said arbitration logic is associated with said read/write port and said arbitration logic is configured to route~~routes~~ a data access request requesting access of data in said first memory portion received from said memory access interface to said first bus and to route~~routes~~ a further data access request requesting access of data in said second memory portion received from said data processing portion to said second bus, said routing of said data access requests being ~~performed~~ performable during the same clock cycle,

wherein said first and second portions of said memory include an instruction portion for storing instructions and at least one data portion for storing data items, respectively, said arbitration logic configured to route said data access request to said first bus for providing access

to said instruction portion when data to be transferred is an instruction and to route said data access request to said second bus for providing access to said at least one data portion when data to be transferred is a data item, and

wherein said at least one data portion includes an even data portion for storing data having an even address and an odd data portion for storing data having an odd address, said read/write port configured to transfer data between said processor core and said at least one memory via three buses including said first bus for providing access to said instruction portion, said second bus for providing access to said odd data portion, and a third bus for providing access to said even data portion, and said arbitration logic is configured to route a data access request to said first bus when data to be transferred is an instruction, to said second bus when data to be transferred is a data item associated with an odd address, and to said third bus when data to be transferred is a data item associated with an even address.

2. (previously presented) A data processing apparatus according to claim 1, said arbitration logic selecting one of said first and second buses to which said data access request is routed in dependence upon an address location within said at least one memory associated with said data access request.

3. Canceled.

4. Canceled.

5. (previously presented) A data processing apparatus according to claim 1, wherein said arbitration logic, in response to receipt of a data access request from said memory access interface portion and a data access request from said data processing portion, both data access requests requesting access to data in one portion of said at least one memory, routing said data access request from said memory access interface portion to one of said first and second buses providing data access to said one portion of said at least one memory before routing said request from said processing portion to said one of said first and second buses.

6. (previously presented) A data processing apparatus according to claim 1, said arbitration logic detecting a wait request from at least one busy portion of said at least one memory, said arbitration logic not routing any data access requests to said busy portion until said wait request is no longer detected.

7. Canceled.

8. (currently amended) ~~A data processing apparatus according to claim 1,~~A data processing apparatus comprising:

arbitration logic; and

a data processor core, said data processor core comprising:

a memory access interface portion for performing data transfer operations between an external data source and at least one memory associated with said data processor core;

a data processing portion for performing data processing operations;

a read/write port for transferring data from said processor core to first and second buses for providing data communication between said processor core and said at least one memory, said at least one memory including first and second memory portions, said first bus providing exclusive access to said first memory portion and said second bus providing exclusive access to said second memory portion, wherein said arbitration logic is associated with said read/write port and said arbitration logic is configured to route a data access request requesting access of data in said first memory portion received from said memory access interface to said first bus and to route a further data access request requesting access of data in said second memory portion received from said data processing portion to said second bus, said routing of said data access requests being performable during the same clock cycle, and

wherein said at least one memory is divided into three portions, an instruction portion for storing instructions, ~~and two data portions,~~ an even data portion for storing data having an even address, and an odd data portion for storing data having an odd address, said data processing apparatus comprising three buses, said read/write port configured to transfer ~~transferring~~ data between said processor core and said at least one memory via said three buses, said first bus for providing access to said instruction portion, said second bus for providing access to said odd data portion, and a third bus for providing access to said even data portion.

9. (original) A data processing apparatus according to claim ~~7~~8, wherein said at least one memory is a tightly coupled memory.

10. (currently amended) A method of transferring data between an external data source and at least one memory associated with a data processor core, said data processor core

comprising a memory access interface portion performing data transfer operations between said external data source and said at least one memory associated with said data processor core and a data processing portion performing data processing operations, said method comprising the steps of:

in response to a data access request requesting access of data in a first memory portion of said at least one memory received from said memory access interface portion and a data access request requesting access to data in a second memory portion of said at least one memory received from said data processing portion, routing said data access request received from said memory access interface portion to one of first and second buses, said first bus providing exclusive access to said first memory portion, and routing said data access request received from said data processing portion to a second bus, said second bus providing exclusive access to said second memory portion, said routing of said data access requests being performed during the same clock cycle,

wherein said first and second portions of said memory include an instruction portion storing instructions and at least one data portion storing data items, said routing said data access requests includes routing a data access request to said first bus providing exclusive access to said instruction portion when data to be transferred is an instruction and routing said data access request to said second bus providing exclusive access to said at least one data portion when data to be transferred is a data item, and

wherein said at least one data portion includes two data portions, an even data portion storing data having an even address and an odd data portion storing data having an odd address, said routing step including routing data accesses to one of three buses, said first bus providing access to said instruction portion, said second bus providing access to said odd data portion, and

a third bus providing access to said even data portion, and said routing including routing a data access request to said first bus when data to be transferred is an instruction, to said second bus when data to be transferred is a data item associated with an odd address, and to said third bus when data to be transferred is a data item associated with an even address.

11. (original) A method according to claim 10, wherein said step of routing data access requests to respective data buses is done in dependence upon an address location within said at least one memory associated with said data access request.

12. Cancelled.

13. Canceled.

14. (original) A method according to claim 10, wherein said routing step in response to receipt of a data access request from said memory access interface portion and a data access request from said data processing portion, both data access requests requesting access to data in a portion of said at least one memory accessed by one of first and second buses, routes said data access request from said memory access interface portion to said one of said first and second buses before routing said request from said processing portion to said one of said first and second buses.

15. (original) A method according to claim 10, said routing step detecting a wait request from at least one busy portion of said at least one memory, and in response to detection of said

wait request not routing any data access requests to said busy portion until said wait request is no longer detected.

16. (currently amended) ~~A method according to claim 10,~~ A method of transferring data between an external data source and at least one memory associated with a data processor core, said data processor core comprising a memory access interface portion performing data transfer operations between said external data source and said at least one memory associated with said data processor core and a data processing portion performing data processing operations, said method comprising:

in response to a data access request requesting access of data in a first memory portion of said at least one memory received from said memory access interface portion and a data access request requesting access to data in a second memory portion of said at least one memory received from said data processing portion, routing said data access request received from said memory access interface portion to one of first and second buses, said first bus providing exclusive access to said first memory portion, and routing said data access request received from said data processing portion to a second bus, said second bus providing exclusive access to said second memory portion, said routing of said data access requests being performed during the same clock cycle,

wherein said at least one memory is divided into three portions, an instruction portion storing instructions, and two data portions, an even data portion storing data having an even address and an odd data portion storing data having an odd address, said routing step routing a received data access request to one of three buses, said first bus providing access to said instruction portion, said second bus providing access to said odd data portion, and a third bus

providing access to said even data portion, in dependence upon an address of said data associated with said data access request.

17. (previously presented) Arbitration logic controlling a data processor to perform the steps of the method according to claim 10.

18. (previously presented) A data processing apparatus according to claim 1, wherein said data processor core comprises said arbitration logic.